

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

By the present Preliminary Amendment the specification is amended to address the objection noted on pages 2 and 4. With respect to the objections noted on pages 1 and 8 those objections were addressed by previously submitted amendments.

Claims 1-11 are pending in this application. Claims 1 and 6 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-11 were rejected under 35 U.S.C. § 102(b) as anticipated by the publication “A Core Generator For Fully Synthesizable And Highly Parameterizable RISC-Cores For System-On-Chip Designs” to Berekovic et al. (herein “Berekovic”).

Addressing first the rejection of claims 1 and 6 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by present response.

Claims 1 and 6 were rejected as the reference to “the method” did not have clear antecedent basis. In reply claims 1 and 6 now refer to “a method”, which is believed to address that rejection.

Addressing now the rejection of claims 1 and 11 under 35 U.S.C. § 102(b) as anticipated by Berekovic, that rejection is traversed by the present response.

Initially, applicants note each of independent claims 1 and 6 is amended by the present response to clarify that in the selecting at least one of a plurality of option instructions, the option instructions “are provided respectively in correspondence with machine instructions to be implemented within said processor core”. No new matter is believed to be raised.

The claims as currently written are believed to clearly distinguish over the applied art.

The outstanding rejection cites Berekovic to teach:

...the soft-cores processors have high flexibility to be configured with arbitrarily chosen parameters by user, such as selecting cache size, selecting a data memory etc. as a fact of inheriting the configuration specifics from the ability of the configuration process of the processors (Pages 562, 563); pages 567-568 also show that selection of cache size (candidates) is selected through parameters, such as data word width.¹

In response to that basis for the outstanding rejection applicants first note Berekovic provides no description of the selection of cache size, even if an instruction RAM and a data RAM are caches. The outstanding Office Action references the selection of cache size related to a data word width. However, in that respect applicants note the cache size (and the memory capacity) can be selected independent from a data word width. The performance of an information processing unit is routinely improved by simply increasing the capacity of a cache. It is also apparent that the opposite may be true. Thus, applicants note that the reliance in the Office Action on the relation between the selection of cache size and a data word width is believed to be improper.

One basis for the outstanding rejection also relies upon Berekovic disclosing “selecting at least one of a plurality of option instructions to be implemented within the processor by developing a soft core generator for highly parametrizable RISC-cores having an option of the of choosing the instruction word width along with parameters being able configured (abstract)”.² In reply to that basis for the outstanding rejection applicants note Berekovic provides no disclosure or suggestion with respect to “option instructions” that are extra instructions that can be used in addition to basic instructions.

In accordance with Berekovic, a program counter (PC) points to a larger memory with a wide word width, and such a wide word from a memory contains a very long instruction work, where the RISC instructions (8, 16, or 32-bit respectively) are also stored. In Berekovic the rest of the instruction is partitioning to multiple, smaller “dedicated”

¹ Office Action of December 6, 2005, the sentence bridging pages 3 and 4.

² Office Action of December 6, 2005, the bottom of page 3.

instructions that serve for the control of multiple function-specific units. Applicants also note that in Berekovic the dedicated instructions are indispensable instructions rather than option instructions that can be introduced to improve performance or that can be dispensed with if unnecessary.

As shown for example in Figure 3 in Berekovic the “dedicated” instructions are stored in a VLIW Instruction RAM in which very-long “horizontal” microcode instructions are stored as dedicated instructions with different instruction lengths. In that case, however, the microcode instructions cannot be considered as machine instructions that are used directly in writing an application program.

Berekovic may use a compiler that can generate RISC instructions (which may be “vertical”) together with very-long horizontal microcode instructions associated with each other, from an application program written by the use of a RISC instruction set made of instructions of a same predefined word width.³

Considering such a complicated configuration in Berekovic, applicants submit the VHDL template file including the very-long horizontal microcode instructions are not option instructions that can be selected by a user of the VHDL system. In fact, Berekovic only describes that the instruction word width, the data path width, and the number of registered files are selectable. Berekovic does not appear to indicate any selectable option instructions.

In contrast to Berekovic, in the claims as currently written a processor designer can designate the use of option instructions selected from among a plurality of such option instructions provided in the HDL system. The selectable configurations are implemented within the system. Particularly, the option instructions are machine instructions that can be easily handled by process designers, and therefore the compiler can be easily provided such that running of an application can be easily evaluated.

³ See Berekovic at page 563.

Applicants also note Berekovic suggests that a division can alternatively be implemented in software, but the use of a dividing option instruction is not at all suggested. Further, applicants note the “implementation” parameters as discussed above in Berekovic are usually low level parameters such as parameters of a design rule, rather than system architecture parameters that are to be particularly discussed such as the instruction word width, the data path width, and the number of registered files.

Independent claims 1 and 6 as currently written, and the claims dependent therefrom, are directed to processors that can provide high performance throughput as compared with background processors that are merely designed on the basis of HDL templates, because of the available option instructions as discussed above. Berekovic does not disclose or suggest the “option instructions” as claimed.

In such ways, the claimed features are believed to clearly distinguish over Berekovic. Thereby, independent claims 1 and 6, and the claims dependent therefrom, are believed to clearly distinguish over Berekovic.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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